REMARKS

Claims 1-28 are pending in the present application. Claims 15-28 are withdrawn from consideration. Claims 1-14 are rejected.

Claim Rejection under 35 U.S.C. §103

Claims 1-12 are rejected under 35 U.S.C. §103(a) as being unpatentable over Hiyama et al. (JP 2000-286396) in view of Tsu et al. (U.S.P. 6,294,420). Claims 13 and 14 are rejected under 35 U.S.C. §103(a) as being unpatentable over Kanaya et al. (U.S. Pub. 2002/0063274) in view of Tsu et al.

Applicants respectfully disagree with the above rejection, because not all of the limitations of the present invention are taught or suggested by the cited reference.

With regard to claims 1, 13 and dependent claims of claim 1, Applicants note that claims 1, 13 and dependent claims of claim 1 have a feature that the buffer structure having a height larger than a width thereof is formed between the substrate and the lower electrode. The width of the buffer structure is narrowed, whereby the influence of the stress caused by the thermal expansion coefficient difference between the substrate and the capacitor dielectric film can be suppressed. The height of the buffer structure is made larger than the width thereof, whereby the propagation of the stress to the capacitor dielectric film can be suppressed. Thus, according to this feature of the present invention, the stress applied to the capacitor dielectric film caused by the thermal expansion

coefficient difference between substrate and the capacitor dielectric film can be suppressed by the buffer structure, whereby the capacitor dielectric film, having a crystal oriented substantially perpendicular to a surface of the lower electrode can be formed. From the viewpoint of controlling the film orientation of the capacitor dielectric film, it is very important to control the relationship between the height of the buffer structure and the width thereof.

Applicants note that Hiyama et al. discloses a buffer layer 3 for controlling the crystal orientation of the lower electrode. However, Hiyama et al. neither teaches nor suggests the buffer structure having a height larger than a width thereof. Hiyama et al. also neither teaches nor suggests the suppression of the stress applied to the capacitor dielectric film caused by the thermal expansion coefficient difference between the substrate and the capacitor dielectric film.

Tsu et al. discloses capacitors having a three-dimensional lower electrode 12. However, Tsu et al. neither teaches nor suggests the buffer structure (22) formed between the substrate and the lower electrode (20). Tsu et al. also neither teaches nor suggests the suppression of the stress applied to the capacitor dielectric film caused by a thermal expansion coefficient difference between the substrate and the capacitor dielectric film. Applicants note that the Examiner regards the element of the reference numeral 12 of Tsu et al. as the buffer structure. However, Applicants respectfully submit that the element of the reference numeral 12 is not the buffer structure but the lower electrode (see column 3, lines 36-39 and Fig. 1). The layers 18 and 20 forming the lower electrode 12 do not have the general functions of the buffer layer, such as suppressing the stress or controlling the film orientation, so that it is impossible to interpret the layers 18 and 20 as the buffer structure. The layers 18 and 20 are parts of only the lower electrode. Similarly, the element of the reference

numeral 3a of Kanaya et al. is not the buffer layer but a part of the lower electrode 3. Tsu et al. and Kanaya et al. neither teach nor suggest the buffer structure for suppressing the stress or for controlling the film orientation.

The Examiner states that it would have been obvious to one of ordinary skill in the art to combine the buffer structure teaching of Tsu et al. with Hiyama et al., because the raised buffer structure would have increased the surface area of the electrode in contact with the capacitor dielectric, and thus it would have increased the capacitance. However, from the viewpoint of increasing capacitance, there is no specific technical meaning in making the height of the buffer structure larger than the width thereof, and the ratio of the height to width does not affect capacitance.

Thus, it would have been unobvious to one of ordinary skill in the art to make larger the height of the buffer layer 3 of Hiyama et al. than the width thereof.

With regard to claims 3, 14 and dependent claims of claim 3, Applicants note that claims 3, 14 and dependent claims of claim 3 have a feature that the lower electrode has a height larger than a width thereof. The width of the lower electrode is narrowed, whereby the influence of the stress caused by the thermal expansion coefficient difference between the substrate and the capacitor dielectric film can be lowered. The height of the lower electrode is made larger than the width thereof, whereby the propagation of the stress to the capacitor dielectric film can be lowered. Thus,

according to this feature of the present invention, the stress applied to the capacitor dielectric film caused by a thermal expansion coefficient difference between the substrate and the capacitor dielectric film is suppressed by the lower electrode, whereby the capacitor dielectric film having a crystal oriented substantially perpendicular to a surface of the lower electrode can be formed. From the viewpoint of controlling the film orientation of the capacitor dielectric film, it is very important to control the relationship between the height of the lower electrode and the width thereof.

Hiyama et al. discloses a lower electrode 4 for controlling the crystal orientation of the lower electrode. However, Hiyama et al. neither teaches nor suggests the lower electrode 4 having a height larger than a width thereof. Hiyama et al. also neither teaches nor suggests the suppression of the stress applied to the capacitor dielectric film caused by a thermal expansion coefficient difference between the substrate and the capacitor dielectric film.

Tsu et al. discloses capacitors having a three-dimensional lower electrode 12. However, Tsu et al. neither teaches nor suggests the lower electrode 4 having a height larger than a width thereof. Tsu et al. also neither teaches nor suggests the suppression of the stress applied to the capacitor dielectric film caused by a thermal expansion coefficient difference between the substrate and the capacitor dielectric film.

In Hiyama et al., the buffer layer 3 is formed beneath the lower electrode 4 so as to control the film orientation of the lower electrode 4. On the other hand, in Tsu et al., the film orientation of the capacitor dielectric film 16 is not controlled and no buffer layer is formed beneath the lower

electrode 12. Thus, the basic structures of these capacitors are clearly different with each other, so that these capacitors cannot be simply combined. For example, when the lower electrode 12 of Tsu et al. is applied to the capacitor of Hiyama et al., the film orientation of the capacitor dielectric film 5 cannot be controlled. Tsu et al. is characterized by forming lower electrode of three-layer structure in self-alignment, and in order to realize this feature, it has prepared the electrical contact at the undersurface of lower electrode 12. Thus, when the lower electrode 4 of Hiyama et al. is solidified like the lower electrode 12 of Tsu et al., it becomes impossible therefore, to take the electrical contact of lower electrode 4 by existence of the insulating buffer layer 3. Therefore, one of ordinary skill in the art does not combine capacitor of Hiyama et al., and capacitor of Tsu et al. Additionally as described above, from the viewpoint of increasing capacitance, there is no specific technical meaning in making the height of the buffer structure larger than the width thereof.

Thus, it would have been unobvious to one of ordinary skill in the art to make larger the height of the lower electrode 4 of Hiyama et al. than the width thereof.

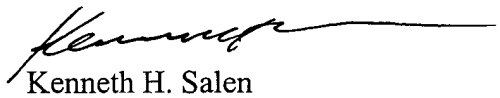
For at least the above reasons, Applicants respectfully submit that the claimed invention defines patentable subject matter. Applicants earnestly request withdrawal of the rejections and passage of the claims to issue.

If the Examiner believes that this application is not now in condition for allowance, the Examiner is requested to contact Applicants' undersigned attorney at the telephone number indicated below to arrange for an interview to expedite the disposition of this case.

In the event that this paper is not timely filed, Applicants respectfully petition for an appropriate extension of time. Please charge any fees for such an extension of time and any other fees that may be due with respect to this paper to Deposit Account No. 01-2340.

Respectfully submitted,

ARMSTRONG, WESTERMAN & HATTORI, LLP



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